Lowercase "or" was ignored. Try "OR" to search for either of two terms. [details]

Scholar All articles - Recent articles Results 1 - 10 of about 16,000 for branch + target + (region or block) + map + entry. (0.43 seconds)

A design space evaluation of grid processor architectures
R Nagarajan, K Sankaralingam, D Burger, SW Keckler - Microarchitecture, 2001. MICRO-34. Proceedings. 34th ACM/ ..., 2001 - ieeexplore.ieee.org
... and destroyed in the pred- icated region (ie, 15 is the only leaf node in the predicated region). ... When a branch executes, and sends its target to the ...
Cited by 143 - Related articles - Web Search - BL Direct - All 6 versions

Entry point mapping and skipping method and apparatus
PL Fu, DE Lenoski - US Patent 5,032,983, 1991 - freepatentsonline.com
... 30 to select a jump address in target register 28 ... In one implementation of a variable skipping region, skipping is done until there is a jump or branch in the ...
Cited by 7 - Related articles - Web Search - All 5 versions

Presbyopic branch target prefetch method and apparatus
H Wang, R Kling, ET Grochowski, K Ramakrishnan - US Patent 6,732,260, 2004 - freepatentsonline.com
... entry location of the first code region to entry ... of claim 23 wherein the presbyopic target buffer is ... in a first buffer that maps branch instruction addresses ...
Cited by 1 - Related articles - Web Search - All 3 versions

Meld Scheduling: A Technique for Relaxing Scheduling Constraints - hp.com [PDF]
SG Abraham, V Kathail, BL Deitrich - International Journal of Parallel Programming, 1998 - Springer
... Since a basic block has only one entry and one ... In a single-entry region, the distance map provides the ... of the schedule time of the exit (branch) operation and ...
Cited by 10 - Related articles - Web Search - BL Direct - All 11 versions

Fast branch misprediction recovery method and system
A Yoaz, G Pribush, F Gabbay, M Erez, R Ronen - US Patent 6,757,816, 2004 - freepatentsonline.com
... to determine its mapping and validity; map and validate ... fields 512 in the alternative branch-target address table ... in the remaining bogus region, block 606 . ...
Cited by 2 - Related articles - Web Search - All 3 versions

A Hierarchical Dependence Check and Folded Rename Mapping Based Scalable Dispatch Stage
V Sankaranarayanan, A Tyagi - Proc. of the IEEE International Conference On Computer Design ..., 2001 - doi.ieeecs.org
... of instructions (relative to the previous branch in- struction ... We stored the target instructions for taken branches in ... program comes to the same region of the ...
Cited by 5 - Related articles - Web Search - Library Search - All 6 versions

Software-Based Transparent and Comprehensive Control-Flow Error Detection
E Borin, C Wang, Y Wu, G Araujo - Code Generation and Optimization, 2006. CGO 2006. ..., 2006 - doi.ieeecomputersociety.org
... Figure 9 - Regions attributed to a basic block. Region R2E/R3E means that R2E and R3E are valid ... branch targets: Definition 1: The logic branch target is the ...
Cited by 18 - Related articles - Web Search - All 4 versions

Introducing the IA-64 Architecture - rose-hulman.edu [PDF]
J Huck, D Morris, J Ross, A Knies, H Mulder, R ... - IEEE MICRO, 2000 - doi.ieeecomputersociety.org
... it also records information such as the target register, memory ... Loop-type branch behavior ... The region registers allow the operating system to concurrently map 8 ...
Cited by 111 - Related articles - Web Search - BL Direct - All 54 versions

A region-based compilation technique for a Java just-in-time compiler
T Suganuma, T Yasue, T Nakatani - Proceedings of the ACM SIGPLAN 2003 conference on ..., 2003 - portal.acm.org
... and the non-rare path in the other branch direction, but ... and estimate the cost for the reduced target code, but ... region exit basic block (RE-BB) object captured ...
Cited by 37 - Related articles - Web Search - BL Direct - All 4 versions

A good antisense molecule is hard to find - unibe.ch [PDF]
AD Branch - Trends in Biochemical Sciences, 1998 - Elsevier
... A, D. Branch is in the Division of Liver Diseases ... virus is considered to be a potential target for antisense ... This short region contains a particular 10-mer that ...
Cited by 274 - Related articles - Web Search - BL Direct - All 5 versions

Key authors: R Nagarajan - R Kessler - S Keckler - A Branch - D Burger

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Scholar All articles - Recent articles Results 1 - 10 of about 9,480 for branch + target + buffer + (region or block) + entry. (0.21 seconds)

Pageable branch history table
JH Pomerene, TR Puzak, RN Rechtschaffen, PL ... - US Patent 4,679,141, 1987 - freepatentsonline.com
... 171, will issue TA on path 127 and cause the I-Buffer to load ... 14. The entry shows
the location (8) of branch #1 in the block and the target address (02E104 ...
Cited by 46 - Related articles - Web Search - All 5 versions

Using branch handling hardware to support profile-driven optimization
TM Conte, BA Patel, JS Cox - Proceedings of the 27th annual international symposium on ..., 1994 - portal.acm.org
... block id in a buffer. This buffer is then parsed into ... The target of the branch is
changed to this new transition block, and an unconditional branch to ...
Cited by 63 - Related articles - Web Search - All 6 versions

Performance Optimization of Pipelined Primary Caches
K Olukotun, T Mudge, R Brown - Computer Architecture, 1992. Proceedings., The 19th Annual ..., 1992 - ieeexplore.ieee.org
... A branch-target buffer (BTB) is a cache whose entries ... the mapping between the basic
block entry points of ... after the branch and from the branch target into the ...
Cited by 29 - Related articles - Web Search - BL Direct - All 5 versions

Instruction prefetch buffer control
VG Oklobdzija, DT Ling - US Patent 4,714,994, 1987 - freepatentsonline.com
... in the art how the instruction prefetch buffer and its ... a successful branch out of
the region was encountered ... 2. Branch successful and branch target is in the ...
Cited by 57 - Related articles - Web Search - All 4 versions

... single array cache memory having first and second storage regions for storing non-branch and branch ...
R Kumar, PG Emerson - US Patent 5,737,750, 1998 - freepatentsonline.com
... to the cache memory 10 is a branch target instruction, then ... prefetch buffer 6 and
the tag buffer 4, respectfully ... be stored to the second storage region 14 of ...
Cited by 15 - Related articles - Web Search - All 3 versions

A study of slipstream processors - ncsu.edu [PDF]
Z Purser, K Sundaramoorthy, E Rotenberg - Proceedings of the 33rd annual ACM/IEEE international ..., 2000 - portal.acm.org
... chains are not confined within a small region. ... D. • Effectively, the branch terminating
block A is ... The processor's branch target buffer may be modified to ...
Cited by 63 - Related articles - Web Search - BL Direct - All 18 versions

Unconstrained speculative execution with predicated state buffering - nagoya-u.ac.jp [PDF]
H Ando, C Nakanishi, T Hara, M Nakaya - Computer Architecture, 1995. Proceedings. 22nd Annual ..., 1995 - ieeexplore.ieee.org
... completes by jumping to the predicted target of the ... every cycle by referring to the
branch conditions. ... predi- cated register file, and predicated store buffer. ...
Cited by 20 - Related articles - Web Search - BL Direct - All 11 versions

Branch Effect Reduction Techniques
AK Uht, V Sindagi, S Somanathan - COMPUTER, 1997 - doi.ieeecs.org
... the size of the average basic block and increasing ... If there is no entry in the buffer,
the branch ... 2-bit automaton's state is stored in a branch target buffer. ...
Cited by 40 - Related articles - Web Search - BL Direct - All 7 versions

... supplying apparatus with a branch target buffer having the contents so updated as to enhance branch ...
T Hara - US Patent 5,740,415, 1998 - freepatentsonline.com
... and sets of the instruction memory 50 and the branch target buffer 20 are identical
to each other, the branch instruction in the region indicated by the ...
Cited by 5 - Related articles - Web Search - All 3 versions

Computer processing unit employing a separate millicode branch history table
PG Emma, JW Knight III, TR Puzak, JR Robinson, AJ ... - US Patent 5,634,119, 1997 - freepatentsonline.com
... of instructions fetched into the instruction buffer 105 from ... This entry contains
the location of the branch instruction and the predicted target address of ...
Cited by 12 - Related articles - Web Search - All 3 versions

Key authors: E Rotenberg - T Conte - D Burger - S Keckler - Z Purser

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